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PATENT ABSTRACTS OF JAPAN

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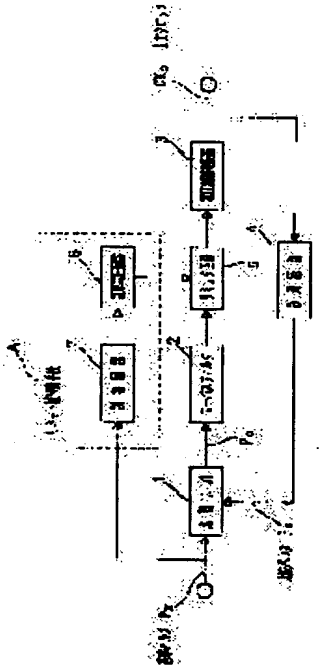
(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : OZAWA KENJI

(54) PLL CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress the malfunction of circuit connected on a rear stage with a phase locked loop (PLL) circuit for the digital signal processing of video signal processing.
SOLUTION: A limiter circuit 5 for limiting the output of low-pass filter(LPF) 2 is interposed between the LPF 2 and a voltage controlled oscillator 3, and a limit value control means A is provided for controlling the limit value of this limiter circuit 5 corresponding to the frequency change of reference pulse PH. Thus, the malfunction of digital processing circuit connected at the back of PLL circuit can be suppressed and the stable time of PLL circuit can be shortened. Further, by switching a limit voltage for each frequency to be switched, the LPF can be easily designed and the stable time of PLL circuit can be optimized as well.



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